

ABSTRACT

A technique to implement removal of dead time control circuitry from the back-end of a digital switching amplifier system 100 and add dead time control circuitry on the front-end digital modulator chip. The front-end dead time control circuitry adaptively
5 adjusts timing of the output PWM control signals 124 to optimize performance and power consumption, i.e. operate with minimum dead time for all transitions. The front-end dead time control circuitry controls all propagation delays associated with the digital switching amplifier system 100.